Remarks

Reconsideration of remaining claims 12-30, 33, 32, 37-52, 55 and 56 is respectfully requested.

In the Office action dated September 9, 2003 (application Paper No. 0803), the Examiner requested a confirmation of a preliminary election in response to a restriction requirement, and presented a substantive rejection of a set of the pending claims. The Examiner's request and rejections will be discussed below in the order appearing in the Office action.

Restriction Requirement under 35 USC 121

In light of a telephonic election made on August 20, 2003, applicant affirms the election - without traverse - to prosecute the invention of Group I (claims 12-30, 33-34, 37-52, and 55-56). It is to be noted claims 1-11 were previously cancelled by virtue of the filing of a Preliminary Amendment in this application.

35 USC § 103(a) Rejection - Claims 12-30, 33-34, 37-52, and 55-56

The Examiner rejected all pending claims under 35 USC 103(a) as being unpatentable over US Patent 6,596,610 (Kuwabara et al.) in view of US Patent 4,403,825 (Tangonan et al.) and US Patent 6,078,707 (Yamamoto et al.). In particular, the Examiner cited Kuwabara et al. as teaching "an optical device formed on a Silicon-On-Insulator (SOI) wafer ..an upper silicon layer formed on the SOI wafer, the upper silicon layer at least partially forming a waveguide and a waveguide mirror formed in the upper silicon layer". The Examiner referenced Kuwabara et al. at column 5, first paragraph and column 10, fifth paragraph as describing this latter teaching.

In response, applicant asserts that Kuwabara et al. is limited in its teaching to a method for "reclaiming" SOI wafers that are used in the processing and formation of semiconductor electronic devices. See, for example, column 8, beginning at line 53, where it states: "[a] silicon wafer reclaimed as described above by any one of the aforementioned methods of the present invention has a uniformly polished surface condition completely similar to that of usual silicon mirror surface wafers. Therefore, it can be used as a raw material wafer of a bonding SOI wafer, and it may also be used as a

silicon wafer for production of usual integrated circuits and so forth". The "delamination" process of Kuwabara et al. results in forming "mirror-like" top and bottom major surfaces on the wafer - the surfaces upon which electronic devices are made, where "mirror-like" flat surfaces are often required for elements such as high quality gate dielectrics. Applicant believes the formation of a "mirror-like" top surface on an SOI wafer as taught by Kuwabara et al. to be distinguishable from the formation of "a waveguide mirror formed in the upper silicon layer [of an SOI wafer]", as defined by the presently rejected claims. Indeed, applicant asserts that Kuwabara et al. does not disclose or suggest the formation of an optical device, in particular, the formation of a "waveguide mirror" in an "upper silicon layer" of an SOI wafer as defined by the rejected claims. In the rejection, the Examiner stated that the formation of such a waveguide "is inherent of the reference in this optical device art". In response, applicant asserts that the Kuwabara et al. reference is not of the "optical device art", but rather of the electronic IC processing art, where the formation of an optical waveguide is not "inherent".

The Examiner further cited Tangonan et al. as teaching "a thin film of glass layer deposited on an SOI wafer to form a waveguide" and concluded that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the silicon layer partially to form a waveguide on an SOI wafer instead of a glass layer in order to form a waveguide". In response, applicant asserts that while the cited Tangonan et al. reference is of the optical device art, the teaching of Tangonan et al. is limited to devices utilizing a piezoelectric base material - such as lithium niobate - and does not disclose or suggest any device structure utilizing the SOI arrangement of the present invention. A "chalcogenide glass" waveguide layer is considered as particular for use with a lithium niobate substrate and cannot be found to render obvious the structure of the present invention, as defined by claim 33-34, which utilize a "glass layer" formed across the upper silicon layer. The "glass layer" of claims 33 and 34 is not used to support optical transmission - the underlying "upper silicon layer" is still used to support optical propagation in accordance with the teachings of the present invention.

The Examiner cited Yamamoto et al. as disclosing the formation of a "waveguide lens" as defined by rejected claims 37 and 52. In response, applicant has reviewed the cited Yamamoto et al. reference and cannot find a disclosure or teaching of the formation

of a lens by etching an upper silicon waveguide layer of an SOI structure. Indeed, both Tangonan et al. and Yamamoto et al. disclose glass-based waveguides, where glass is used for visible wavelengths. The subject matter of the present invention is directed to the use of silicon-based waveguides, where silicon is transparent only in the infrared wavelength spectrum.

Based upon all of these differences, applicant believes that the pending claims cannot be found to be rendered obvious by the combination of Kuwabara et al., Tangonan et al. and Yamamoto et al. Applicant therefore respectfully requests the Examiner to reconsider this rejection and find all pending claims to be in condition for allowance.

If for some reason or other the Examiner does not believe that the case, in its present form, is ready to issue, the Examiner is invited to contact applicant's attorney at the telephone number listed below.

Respectfully submitted,

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